05-19-05

Cof C

10/846235

Express Mail Label No. Dated: _____

Docket No.: 08211/1200892-US1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Robert C. Taft et al.

Patent No.: 6,847,320

Issued: January 25, 2005

Certificate
MAY 23 2005
of Correction

For: ADC LINEARITY IMPROVEMENT

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322

MS Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted an error which should be corrected.

In the Specification:

Column 1, Line 35, After "present" insert -- invention has been made. --.

Column 3, Line 22, After "further" insert -- averaging and interpolation resistors. --.

Column 4, Line 30, Delete "corrected" and insert -- connected --.

Column 5, Line 7, Delete "(V_{cal})" and insert - - (V_{cal}) - -.

The error was not in the application as filed by applicant; accordingly no fee is required.

Enclosed please find copies of pages 1, 4, 6 & 7.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: May 13, 2005

Respectfully submitted,

By_____

Flynn Barrison
Registration No.: 53,970
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(212) 527-7700
(212) 527-7701 (Fax)
Attorneys/Agents For Applicant

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,847,320

APPLICATION NO. : 10/816,235

ISSUE DATE : January 25, 2005

INVENTOR(S) : Robert C. Taft et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

Column 1, Line 35, After "present" insert -- invention has been made. --.

Column 3, Line 22, After "further" insert -- averaging and interpolation resistors. --.

Column 4, Line 30, Delete "corrected" and insert -- connected --.

Column 5, Line 7, Delete "(V_{cal})" and insert - - (V_{cal}) - -.

Express Mail Label No. Dated: _____

MAILING ADDRESS OF SENDER:
Flynn Barrison
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257

D&D No. 08211/1200892-US1

ADC LINEARITY IMPROVEMENT

Related Application

This application claims the benefit of U.S. Provisional Application Serial No. 60/544,660 filed February 13, 2004, the benefit of the earlier filing date of which is hereby claimed under 35 U.S.C. § 119 (e).

Field of the Invention

The present invention relates to analog-to-digital conversion, and, in particular, to a circuit and method for improvement of linearity in a folding or a flash type analog-digital-converter.

Background

An analog-digital-converter (ADC) is employed to change/convert an analog input signal into a digital output signal. There are several different types of ADC architectures in current use, including pipeline, flash and folding. In a flash ADC, k bits of resolution employ 2^k comparators to convert an analog signal into a digital signal. Folding ADCs are a variation of a typical flash ADC architecture except that they are arranged to map the analog input signal range into N regions where each of these N regions share the same comparators. In a folding ADC, the total number of comparators is typically $2^k/N + (N-2)$.

Flash and folding ADCs may be scaled to very high conversion speeds, since they do not use decision feed-back loops. These two architectures, unfortunately, can be sensitive to device mismatch, leading to linearity degradation. This is especially true of CMOS folding ADCs, since CMOS devices have larger offsets than bipolar devices.

Thus, it is with respect to these considerations and others that the present invention has been made.

Between an input track & hold (sample & hold) circuit and comparator circuit of an ADC, there may be multiple levels of pre-amplification. The first bank of amplifiers may have their output averaged to reduce the effect of offset errors. An amplifier with a large offset is pulled into line by neighboring amplifiers using the resistors tying their outputs together. The second bank also has averaging. However, due to the signal being amplified by the first amplifier before going into the second amplifier, the effect of averaging is much less. An offset in one of the first bank amplifiers creates a broad peak in the ADC's transfer characteristic, and an offset in one of the second bank amplifiers creates a sharp peak. Cascading of the arrayed amplifier banks results in their offsets being added, but with a different shape.

FIGURE 1 schematically illustrates an exemplary embodiment of pre-amplification circuit 100 of a folding ADC. Pre-amplification circuit 100 is configured to receive a single-ended analog signal (V_{IN}) at an input of amplifiers 102 and 106. Amplifiers 102 and 106 are representative of a number of amplifiers forming first bank of amplifiers. Total number of amplifiers in the first bank of amplifiers is determined based, in part, on a desired resolution of a digital output signal of the ADC.

Outputs of representative amplifiers 102 and 106 are connected through averaging resistor $R_{avg, N}$ between nodes 152 and 154. Nodes 152 and 154 are further connected to adjustment resistor $R_{adj, N}$. Adjustment resistor $R_{adj, N}$ is further connected to an input of representative amplifier 104 of second bank of amplifiers. An output of amplifier 104 is connected through averaging resistors to the outputs of other amplifiers in the second bank of amplifiers. Node 156, which connects the output of amplifier 104 and two interpolation resistors is further connected to output 122. Output 122 is connected to an input of a comparator circuit (not shown).

The above described connection of representative amplifier 102 through node 152, adjustment resistor $R_{adj, N}$, and amplifier 104 to the output, is repeated for amplifiers 106 and 108 with adjustment resistor $R_{adj, N-1}$. As mentioned above amplifiers 106 and 108 are connected to other amplifiers in their respective banks through further averaging and interpolation resistors.

FIGURE 3 illustrates a more detailed schematic of one embodiment of folding amplifier triplet 300 in accordance with the present invention, such as those in 2nd amplifier bank in FIGURE 2. Folding amplifier triplet 300 includes current sources 308 and 310 connected to parallel transistor pairs 302, 304, 306. Averaging resistors $R_{avg, N+}$, $R_{avg, N-}$, and the like, connect inputs of individual transistors in amplifier triplet 300 (only one set of averaging resistors shown). Current sources 312, 314, 316 connect the transistor pairs to ground. Each transistor in transistor pairs 302, 304, 306 has a series adjustment resistor, $R_{adj, N,+}$, $R_{adj, N-1,+}$, and the like, coupled to its input. Adjustment currents $I_{adj, N-1,-}$ and $I_{adj, N-1,-}$ (not shown) are injected through adjustment resistors $R_{adj, N,+}$ and $R_{adj, N,-}$. The outputs of transistor pairs 302, 304, 306 are connected through folding bus 320 to an input of a comparator in a comparator circuit. In one embodiment all three transistor pairs are coupled to a single comparator. In another embodiment a ratio of amplifiers to comparators may be determined based, in part, on a desired resolution of a digital output signal of the ADC.

FIGURE 4 schematically illustrates an exemplary embodiment of pre-amplification circuit 400 of a flash ADC. Pre-amplification circuit 400 is configured to receive a single-ended analog signal at input 420 of amplifiers 402, 406, and 410. Amplifiers 402, 406, and 410 are representative of a number of amplifiers forming first bank of amplifiers. The total number of amplifiers in the first bank of amplifiers is determined based, in part, on a desired resolution of a digital output signal of the ADC.

The outputs of representative amplifiers 402 and 406 are connected through averaging resistor $R1_{avg, N}$ between nodes 452 and 454. Node 452 is further connected to adjustment resistor $R_{adj, N}$. Adjustment resistor $R_{adj, N}$ is further connected to an input of representative amplifier 404 of second bank of amplifiers. An output of amplifier 404 is connected through node 456, which connects the outputs of other amplifiers in the second bank of amplifiers through averaging resistors, to output 422. Output 422 is connected to an input of a comparator circuit (not shown).

The above described connection of representative amplifier 402 through node 452, adjustment resistor $R_{adj, N}$, and amplifier 404 to the output, is repeated for amplifiers 406 and 408 with adjustment resistor $R_{adj, N-1}$. As mentioned above amplifiers

406 and 408 are connected to other amplifiers in their respective banks through further averaging resistors.

In one embodiment an analog signal (V_{IN}) is provided to the first bank of amplifiers through input 420 from a track-and-hold circuit (not shown). The signal is processed in pre-amplification circuit 400 as described in FIGURE 1, and provided to the comparator circuit, wherein the injection of adjustment current $I_{adj,\,N}$ through adjustment resistor $R_{adj,\,N}$ provides a relatively flat analog-to-digital transfer curve for the flash ADC employing pre-amplification circuit 400. In another embodiment pre-amplification circuit 400 may have at least one additional bank of amplifiers between the first bank and the second bank. In yet another embodiment, the additional bank of amplifiers may have additional averaging resistors and adjustment resistors similar to the configuration described above. It is understood that all embodiments described here may be implemented for a differential signal as well.

FIGURE 5 illustrates a block diagram of one embodiment of the inventive analog-to-digital converter circuit (500). Circuit 500 includes several components such as a multiplexer (MUX) 592, an optional track-and-hold circuit 582, a pre-amplification circuit 584, a comparator circuit 586, a measurement-and-calibration circuit 580, and a calibration reference circuit 588. FIGURE 5 shows the particular arrangement of inputs and outputs of the various components. In one embodiment, all of the components of circuit 500 are included in the same chip. Alternatively, one or more of the components of circuit 500 may be off-chip.

According to one embodiment, the ADC is calibrated at first power-on. An analog calibration signal (V_{Cal}) is provided to track-and-hold circuit 582 from calibration reference circuit 588. Measurement-and-calibration circuit 580 compares an output 590 of each comparator in comparator circuit 586 to an expected comparator output determining whether an adjustment current injected through the adjustment resistors in pre-amplification circuit 584 needs to be increased or decreased reducing total offset error in pre-amplification circuit 584. After each determination, measurement-and-calibration circuit 580 causes calibration reference circuit 588 to

Application No. (if known): 10/816,235 Attorney Docket No.: 08211/1200892-US1

Certificate of Express Mailing Under 37 CFR 1.10

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail, Airbill No. EU441162879-US in an envelope addressed to:

MS Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on May 13, 2005
Date

B.W. Lee
Signature

B.W. LEE
Typed or printed name of person signing Certificate

Registration Number, if applicable

Telephone Number

Note: Each paper must have its own certificate of mailing, or this certificate must identify each submitted paper.

Certificate of Correction (1 page)
Request for Certificate of Correction (2 pages)
Copies of pages 1,4,6 and 7
Return Postcard